CS 31 Homework 7 Version 2: Set Associative Caches

Due 11:59pm on Thursday, November 13

Full Names:

In this assignment, you will be tracing memory accesses for a set associative cache. Assume the following architecture characteristics:

- 8-bit memory addresses
- 2-byte cache block size
- The cache is 2-way set associative with a total of 4 sets

Question 1

How many bytes of data can be stored in the cache? Do not include metadata like the tag, dirty bit, valid bit, or LRU bit.

Question 2

How are the index bits used in a set associative cache?

How are the tag bits used in a set associative cache?

Question 3

Divide the following two addresses into their `tag`, `index` and `byte offset` parts.

`1 0 1 0 1 0 1 0`   `0 0 1 1 1 0 1 1`

Question 4

On the diagram of the set associative cache on the next page, show the results of the following memory operations (R: read, W: write). Within each box, time should progress downward, so the first address loaded appears at the top and subsequent changes are written below. To the right of the table, label each change with number of the operation that caused it. Assume that an LRU value of 0 means the left line in the set was least recently used and that 1 means the right line was used least recently.

Additionally, annotate each operation below indicating if it is a *hit* or *miss*, and if it caused something else to be evicted from the cache enter *Yes* under *replaced?* otherwise enter *No*. Also, if it caused a block to be evicted and if the evicted block needed to be written back to memory enter *Yes* under *writeback?* otherwise enter *No*.

		hit or miss?	replaced? (No/Yes)	writeback? (No/Yes)
1. R	0 0 0 1 1 0 1 0	___________	_________	_________
2. W	0 0 0 1 1 0 1 1	___________	_________	_________
3. R	1 1 1 1 1 0 0 0	___________	_________	_________
4. R	1 1 1 1 1 0 1 0	___________	_________	_________
5. W	0 1 1 0 1 0 0 0	___________	_________	_________
6. W	0 0 0 0 1 0 0 1	___________	_________	_________
7. R	0 1 1 0 1 0 0 0	___________	_________	_________
8. W	0 0 0 1 1 0 1 0	___________	_________	_________

set	LRU	D	V	tag	D	V	tag
	1	1	1	1 1 1 0 0	1	0	1 0 1 0 1
0							
	0	0	0	1 1 1 1 1	0	0	0 1 0 1 1
1							
	0	0	0	1 0 1 1 1	0	1	0 0 0 0 0
2							
	1	0	1	0 0 0 0 0	0	0	1 0 1 1 1
3							