CS 31 Homework 6: Direct mapped cache (due Nov 6)

Names:

Answer these questions for direct-mapped cache, given a system with:

- 8-bit memory addresses
- 2-byte cache block size
- 4 cache lines

Question 1

How many bytes of data can be stored in the cache? Do not include metadata like the tag or valid bit.

Question 2

How are the tag bits used in a direct mapped cache?
How are the byte offset bits used in a direct mapped cache?

Question 3

Divide the following two sets of address bits into the `tag` and `byte offset`:

`1 0 1 0 1 1 0 0` `0 0 1 1 1 1 0 1`

Question 4

On the diagram of the Direct Mapped Cache on the next page, show the results of the following memory operations (R: read, W: write). Within each box, time should progress downward, so the first address loaded appears at the top and subsequent changes are written below. To the right of the table, label each change with number of the operation that caused it. Don't forget to update the dirty and valid bits! Additionally, annotate each operation below indicating if it is a *hit* or *miss*, and if it caused something else to be evicted from the cache enter *Yes* under *replaced?*, otherwise enter *No*.

	hit or miss?	replaced? (Yes/No)
1. R 0 0 1 0 1 0 1 0		
	----------	----------
2. W 0 0 1 0 1 0 1 1		
	----------	----------
3. R 1 1 0 0 1 1 0 0		
	----------	----------
4. R 1 1 0 0 1 0 1 0		
	----------	----------
5. R 1 1 0 0 1 0 1 1		
	----------	----------
6. W 0 0 1 1 1 1 0 1		
	----------	----------
7. R 0 0 1 1 1 1 0 0		
	----------	----------
8. W 0 0 1 0 1 1 0 0		
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Table 1: Direct Mapped Cache

index	dirty	valid	tag
0	0	0	
1	0	0	
2	0	0	
3	0	0	