

CS31 Written Homework 7: Set Associative Caching

In this assignment, you will be tracing memory accesses for a set associative cache. Assume the following architecture characteristics:

- 8-bit memory addresses
- 2-byte cache block size
- The Cache 2-way Set Associative, with a total of 4 sets.

Question 1

How many bytes of data can be stored in the cache? Do not include metadata like the tag, dirty bit, valid bit, or LRU bit.

Question 2

How are the set bits used in a set associative cache?

How are the tag bits used in a set associative cache?

Question 3

Divide the following address bits into their **set**, **tag** and **byte offset** parts.

1 0 1 0 1 0 1 0

0 0 1 1 1 0 1 1

Question 4

On the diagram of the Set Associative Cache on the next page, results of the following memory operations (R: read, W: write). Within each box, time should progress downward, so the first address loaded appears at the top and subsequent changes are written below. To the right of the table, label each change with number of the operation that caused it. Annotate each operation below with *hit* or *miss* to indicate whether the data were found in the cache. Don't forget to update the dirty, valid, and LRU bits!

1. R 0 0 0 1 1 0 1 0

5. R 0 1 1 0 1 0 0 0

2. W 0 0 0 1 1 0 1 1

6. W 0 0 0 0 1 0 0 1

3. R 1 1 1 1 1 0 0 0

7. R 0 0 0 0 0 0 0 0

4. R 1 1 1 1 1 0 1 0

8. W 0 0 0 1 1 0 1 0

set	LRU	D	V	tag	D	V	tag
0	1		0			0	
1	0		0			0	
2	0		0			0	
3	1		0			0	