Names and Roles:

**Question 1**

For each of the following IA32 instructions, indicate whether the instruction could cause a page fault, whether it could cause a cache miss, and whether it could cause the dirty bit in the cache to be set to 1.

(a) \texttt{movl (}\%eax\texttt{), }\%ebx

\begin{tabular}{c|c|c}
Page fault? & YES or NO & Cache miss? YES or NO & Dirty bit? YES or NO \\
\end{tabular}

(b) \texttt{movl 7, }\%ecx

\begin{tabular}{c|c|c}
Page fault? & YES or NO & Cache miss? YES or NO & Dirty bit? YES or NO \\
\end{tabular}

(c) \texttt{movl 7, (}\%edx\texttt{)}

\begin{tabular}{c|c|c}
Page fault? & YES or NO & Cache miss? YES or NO & Dirty bit? YES or NO \\
\end{tabular}

(d) \texttt{addl -8(}\%eax\texttt{), }\%ebx

\begin{tabular}{c|c|c}
Page fault? & YES or NO & Cache miss? YES or NO & Dirty bit? YES or NO \\
\end{tabular}
For the next three questions you will be tracing memory accesses in a system with the following architecture:

- 8-bit virtual addresses
- 16-byte page size
- 4 pages of physical RAM

**Question 2**

How many bytes of data can a single process store in:

(a) physical memory
(b) virtual memory

**Question 3**

For each the given virtual addresses, divide the address into the page number and page offset.

<table>
<thead>
<tr>
<th>Address</th>
<th>Page Number</th>
<th>Page Offset</th>
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<tbody>
<tr>
<td>10001010</td>
<td>10001111</td>
<td>10101010</td>
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**Question 4**

On the accompanying Page Table diagram, show the results of the following memory operations on RAM and the Page Table. Assume first-in-first-out replacement. Within each box, time should progress downward, so the first address loaded appears at the top and subsequent changes are written below. To the right of the table, label each change with number of the operation that caused it. Annotate each operation below with hit or page fault to indicate whether the data was found in physical memory. Don’t forget to update the valid bits, especially when a page is kicked out!

1. read 00011010
2. write 00011011
3. read 11111000
4. read 11111010
5. read 01101000
6. write 00001001
7. read 00000000
8. read 01010111
9. write 00011010
10. read 00011101
Table 1: Page Table

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<tr>
<th>index</th>
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</tbody>
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